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Sherry et al.

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(54) **HIGH FREQUENCY OSCILLATOR**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**

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H03L 7/099	(2006.01)
H03B 27/00	(2006.01)
H03L 7/23	(2006.01)

(52) **U.S. Cl.**

CPC ***H03K 3/0315*** (2013.01); ***H03B 27/00*** (2013.01); ***H03L 7/099*** (2013.01); *H03L 7/23* (2013.01)

(58) **Field of Classification Search**

CPC H03L 27/00; H03L 7/099; H03L 7/23; H03K 3/0315

USPC 331/57, 74, 2, 46, 185, 45; 327/156, 327/158

See application file for complete search history.

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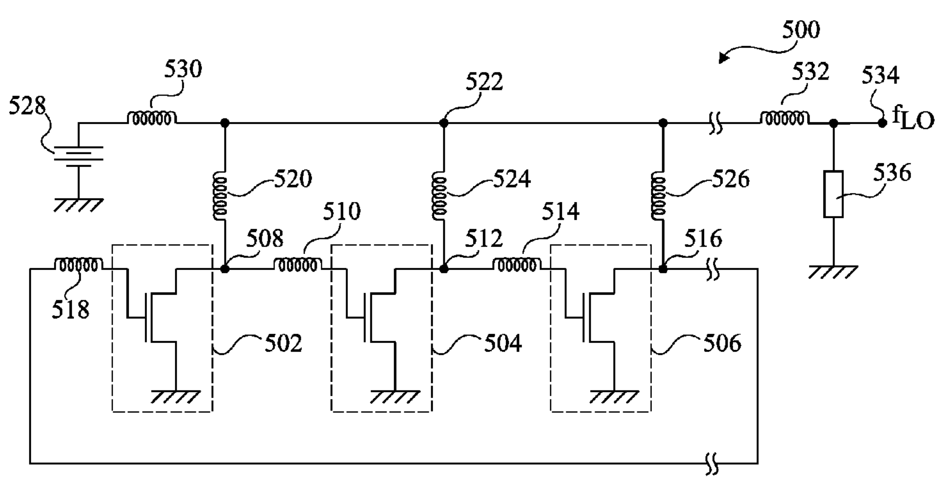
(57) **ABSTRACT**

A frequency oscillator includes a ring oscillator having N inverters coupled in series, where N is an odd integer equal to three or more. A first filter is coupled between an output node of a first of the inverters and an output line of the frequency oscillator. A second filter is coupled between an output node of a second of the inverters and the output line of the frequency oscillator.

21 Claims, 4 Drawing Sheets



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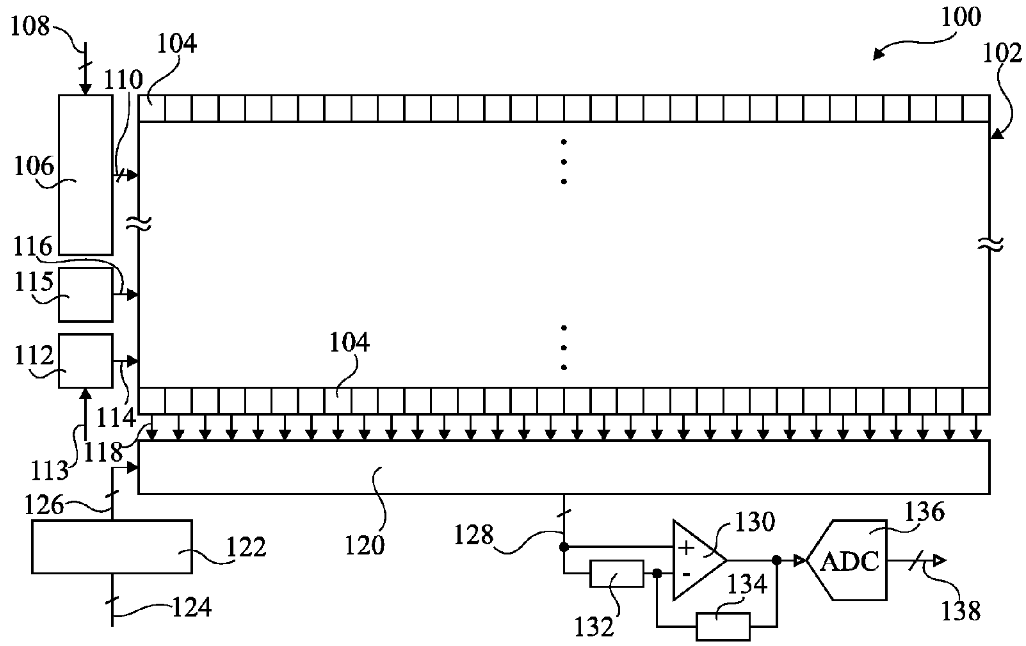
100
102
104
106
108
110
112
113
114
115
116
118
120
122
124
126
128
130
132
134
ADC
136
138

Fig 1

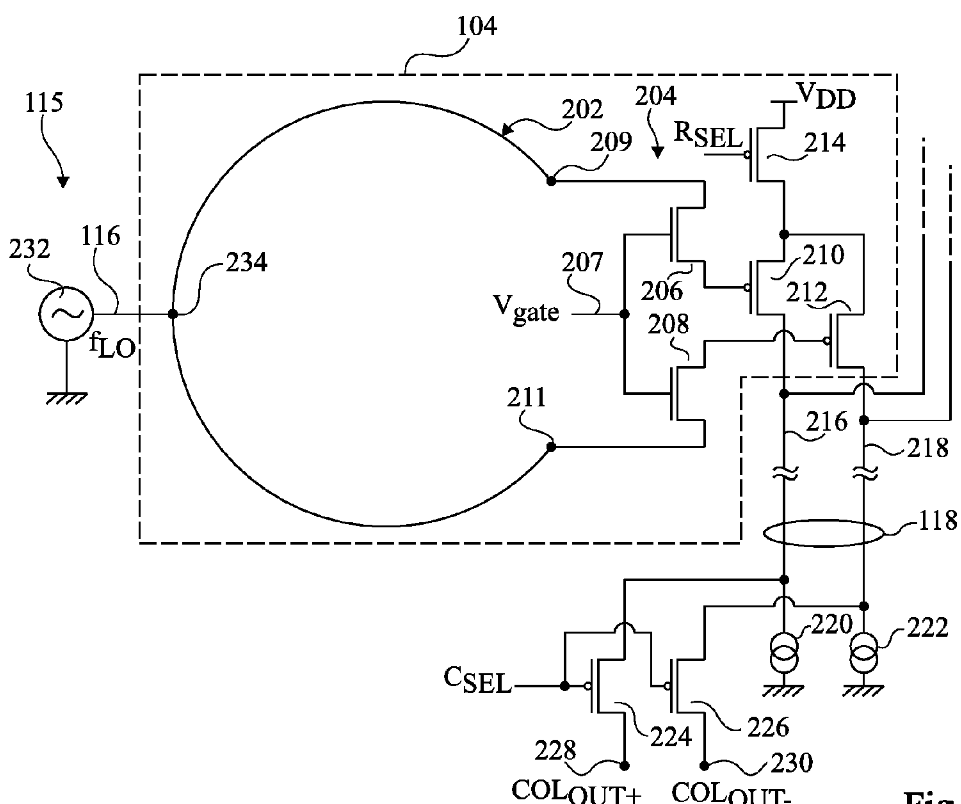
104
115
202
204
V_{DD}
R_{SEL}
214
209
232
116
234
207
206
210
212
V_{gate}
208
f_{LO}
211
216
218
118
220
222
C_{SEL}
224
226
228
230
COL_{OUT+}
COL_{OUT-}

Fig 2

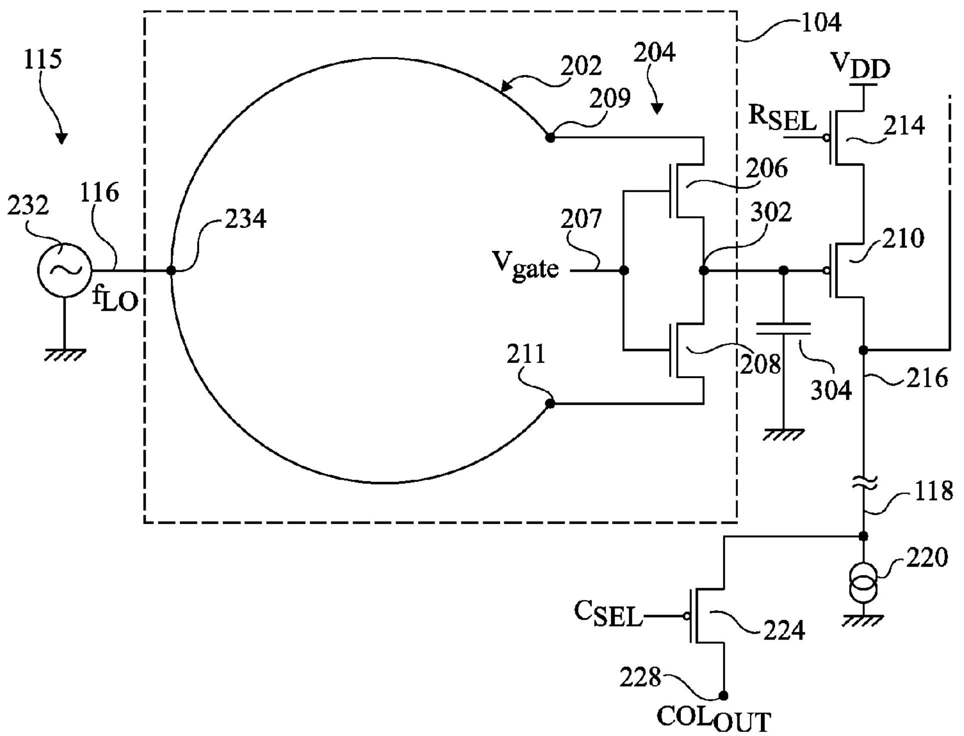
104
115
202
204
209
V_{DD}
R_{SEL}
214
206
232
116
234
207
302
210
f_{LO}
V_{gate}
211
208
304
216
118
220
C_{SEL}
224
228
COL_{OUT}

Fig 3

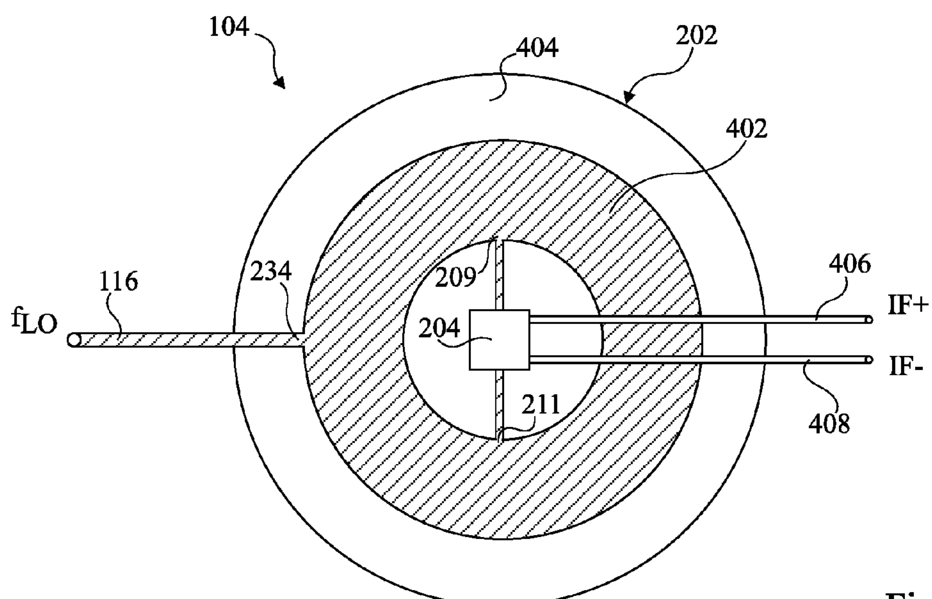
104
404
202
402
116
234
209
406
IF+
f_{LO}
204
IF-
211
408

Fig 4

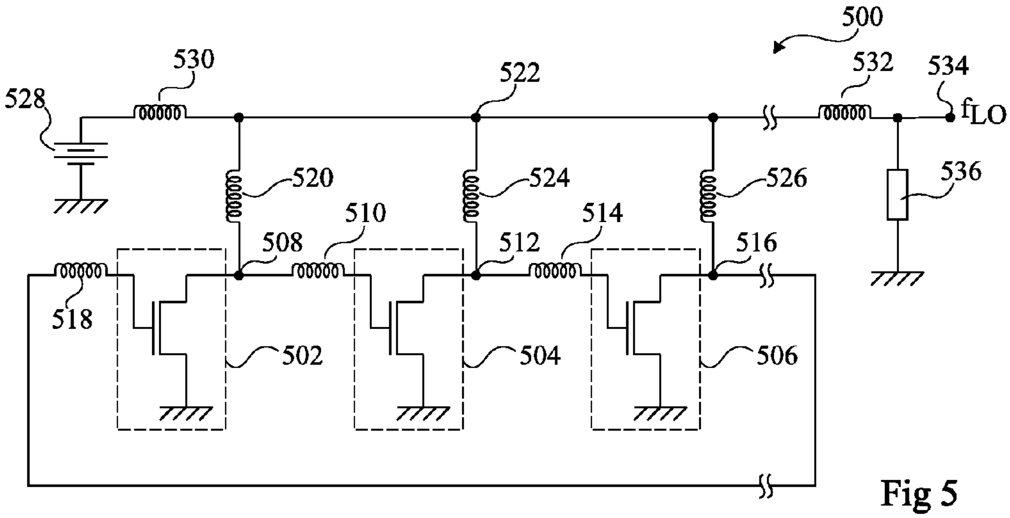

Fig 5

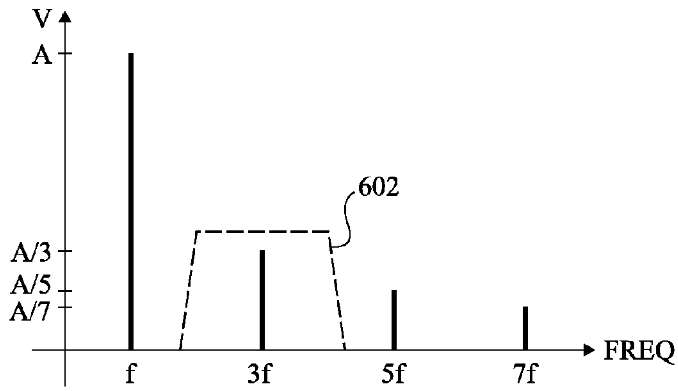

Fig 6

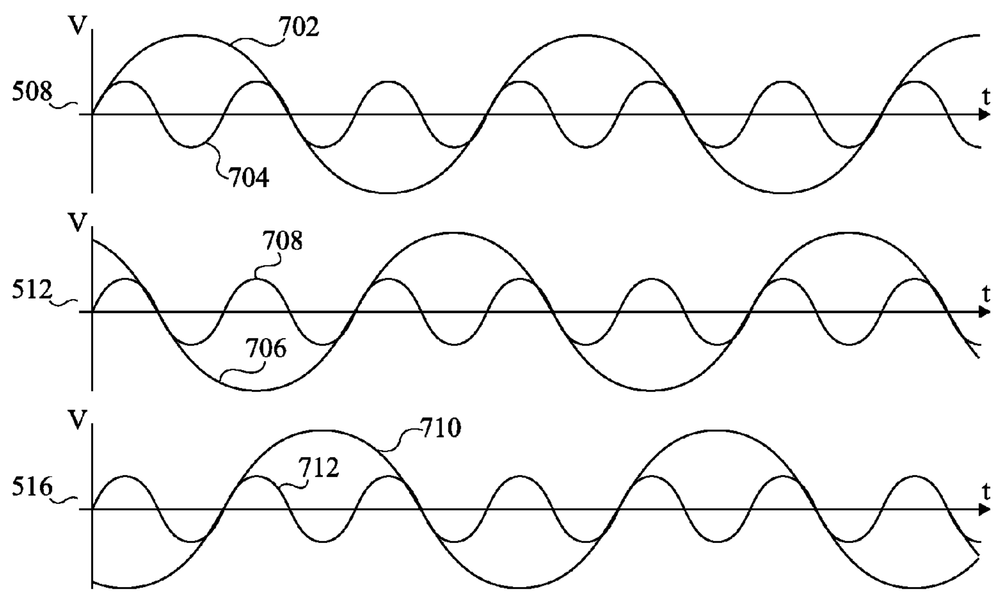

Fig 7

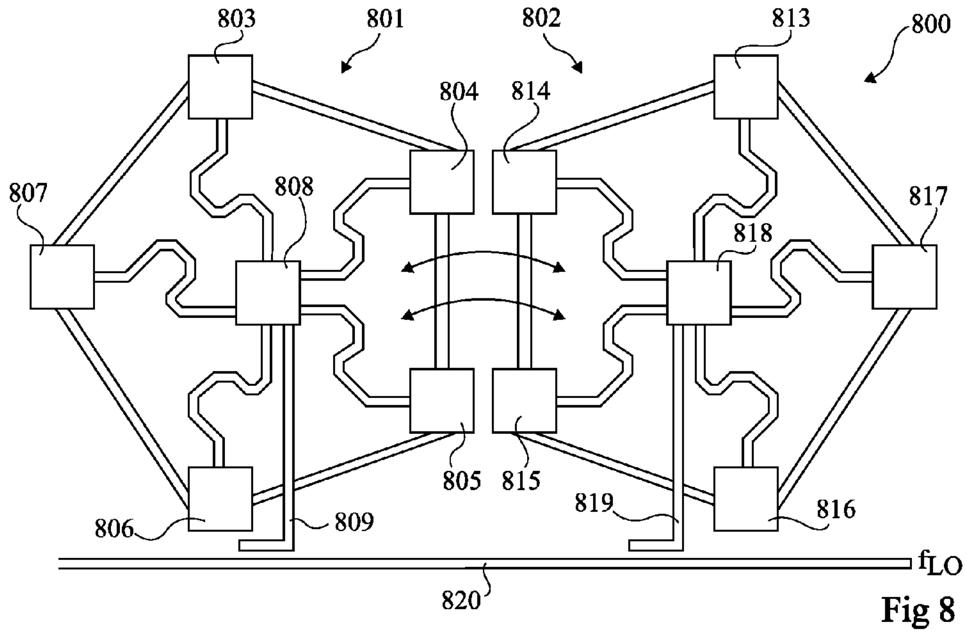

Fig 8

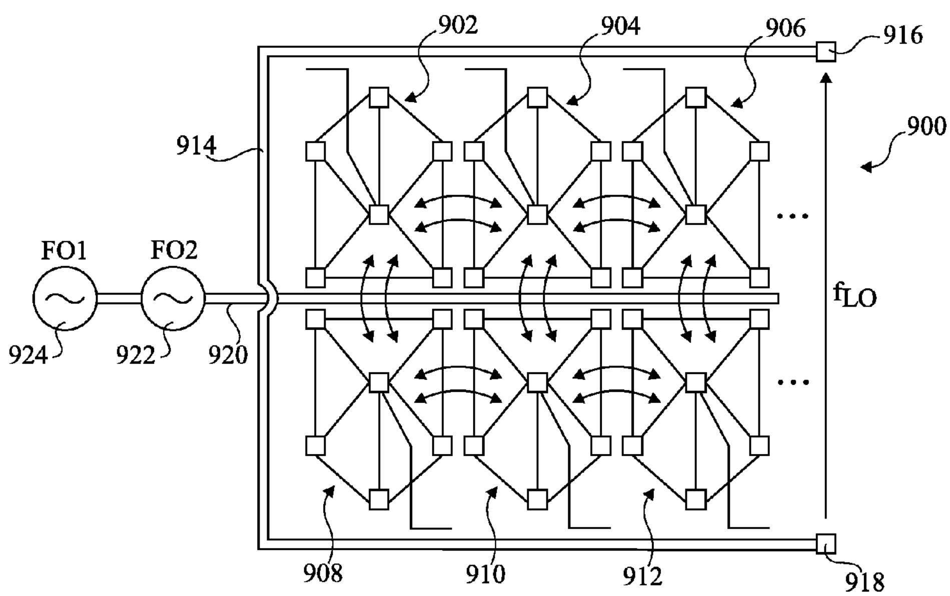

Fig 9

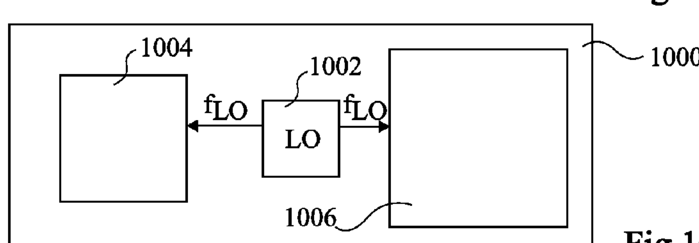

Fig 10

HIGH FREQUENCY OSCILLATOR

This application claims priority to French Patent Application 1258572, which was filed Sep. 12, 2012 and is incorporated herein by reference.

TECHNICAL FIELD

The present disclosure relates to the field of high frequency oscillators, and in particular to a frequency oscillation circuit and method of generating a terahertz signal.

BACKGROUND

A terahertz imager is an image sensor adapted to capture an image of a scene based on waves in the terahertz frequency range. In general, terahertz waves are considered to comprise waves having a frequency of between 300 GHz and 3 THz. These frequencies for example correspond to wavelengths of one millimeter or less. For example, a 1 THz wave has a wavelength of approximately 300 μm.

Terahertz imagers are used widely for applications in which it is desirable to "see through" certain materials. In particular, terahertz waves have good penetrability in many dielectric materials and non-polar liquids. They are however almost entirely reflected by metals and absorbed by water molecules. This makes terahertz imagers particularly suited for applications such as in the security scanners used at airports and in devices used to analyze works of art. The wavelength is in general short enough to achieve good spectral resolution for imaging, but long enough such that the waves are scattered relatively little by air particles such as dust or smoke.

In general, terahertz imagers use a terahertz source to illuminate the scene to be captured. This is because the presence of natural terahertz radiation is generally relatively low.

It has been proposed to provide a fully integrated terahertz camera based on silicon technology. However, there are technical difficulties in implementing such a camera, due at least in part to the relatively high frequency of the terahertz signal range, and the relatively low energy of the signal to be captured. Furthermore, it would be desirable to adapt terahertz imagers to permit them to additionally capture image depth and/or to improve the image quality.

SUMMARY OF THE INVENTION

Embodiments of the present disclosure at least partially address one or more problems in the prior art.

According to one aspect, a frequency oscillator comprises a ring oscillator having N inverters coupled in series, where N is an odd integer equal to three or more. A first filter is coupled between an output node of a first of the inverters and an output line of the frequency oscillator. A second filter is coupled between an output node of a second of the inverters and the output line of the frequency oscillator. For example, the first and second filters are each adapted to filter out at least the fundamental frequency component present at the output nodes of the first and second inverters.

According to one embodiment, the first and second filters have cut-off frequencies selected based on the frequency of the Nth harmonic present at the outputs of the inverters.

According to another embodiment, the first and second filters each have a lower cut-off frequency falling between the (N−2)th and the Nth harmonic present at the outputs of the inverters and a higher cut-off frequency falling between the Nth and (N+2)th harmonic present at the outputs of the inverters.

According to another embodiment, the frequency oscillator further comprises a second ring oscillator formed of N inverters coupled in series, wherein at least one line connecting a pair of inverters of the first ring oscillator is positioned to be electro-magnetically coupled to at least one line connecting a pair of inverters of the second ring oscillator.

According to another embodiment, N is equal to 5 or 7.

According to another embodiment, the first filter comprises a first inductor and the second filter comprises a second inductor.

According to another embodiment, an output of at least one of the N inverters is coupled to the input of the next inverter via a further inductor.

According to another embodiment, a frequency signal on the output line has a frequency in the range of 300 GHz to 3 THz.

According to a further aspect, a method of generating a frequency signal includes generating an oscillating signal by a ring oscillator having N inverters coupled in series, where N is an odd integer equal to three or more. The oscillating signal is generated at the output of each of the inverters. The oscillating signals at the output of at least two of the inverters are filtered to extract the Nth harmonic and the filtered oscillating signals are combined to generate an output frequency signal.

According to one embodiment, the method further comprises generating, by a further ring oscillator having N inverters coupled in series, an oscillating signal at the output of each of the inverters. At least one line connecting a pair of inverters of the first ring oscillator is positioned to be electro-magnetically coupled to at least one line connecting a pair of inverters of the second ring oscillator. The oscillating signal is filtered at the output of at least two of the inverters of the further ring oscillator to extract the Nth harmonic. The filtered oscillating signals of the further ring oscillator are combined with the filtered oscillating signals of the ring oscillator to generate the output frequency signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other purposes, features, aspects and advantages of the invention will become apparent from the following detailed description of embodiments, given by way of illustration and not limitation with reference to the accompanying drawings, in which:

FIG. **1** illustrates a terahertz imager according to an example embodiment of the present disclosure;

FIG. **2** illustrates a pixel circuit of a pixel array of the terahertz imager of FIG. **1** in more detail according to an example embodiment of the present disclosure;

FIG. **3** illustrates a pixel circuit of a pixel array of the terahertz image sensor of FIG. **1** in more detail according to a further example embodiment of the present disclosure;

FIG. **4** illustrates in plain view an antenna of the pixel circuit of FIG. **2** according to an example embodiment of the present disclosure;

FIG. **5** illustrates a frequency oscillation circuit according to an example embodiment of the present disclosure;

FIG. **6** is a graph representing a frequency spectrum of signals in the circuit of FIG. **5** according to an example embodiment of the present disclosure;

FIG. **7** illustrates signals in the circuit of FIG. **5** according to an example embodiment of the present disclosure;

FIG. 8 illustrates a frequency oscillation layout structure according to a further example embodiment of the present disclosure;

FIG. 9 illustrates a frequency oscillation circuit according to yet a further example embodiment of the present disclosure; and

FIG. 10 illustrates a terahertz device according to an example embodiment of the present disclosure.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

FIG. 1 schematically illustrates a terahertz imager **100** according to an example embodiment.

The imager **100** comprises an image sensor formed of a 2-dimensional array **102** of pixel circuits **104**. In the example of FIG. **1**, the array **102** comprises 1024 pixel circuits arranged in 32 rows and 32 columns. Of course, it will be apparent to those skilled in the art that the pixel array **102** could be of a different size and/or aspect ratio. For example, the array **102** could comprise between 2 and several hundred rows and between 2 and several hundred columns of pixels.

The pixel array **102** is for example controlled in a similar fashion to the pixel array of a visible light image sensor. In particular, a row decoder **106** is for example provided, which receives a row selection signal on an input line **108**. The row selection signal indicates a row to be read during a read phase of the pixel array **102**. The row decoder **106** provides a corresponding control signal to a row line (not illustrated in FIG. **1**) of each row of the pixel array **102**. For example in the case that there are 32 rows, the row selection signal is 5 bits wide.

A control block **112** is also for example provided, which receives a control signal on input line **113** for controlling the timing of a global shutter of the pixel array, as will be described in more detail below. The control block **112** provides a corresponding control signal on an output line **114** to each pixel circuit **104** of the pixel array **102**.

Furthermore, as will be described in more detail below, a frequency oscillator circuit **115**, which may be positioned on-chip or off-chip, for example supplies a frequency signal to each pixel circuit **104** of the pixel array **102**.

The pixel array **102**, for example, provides output signals on outputs **118**, each comprising one or more column lines associated with each column of the pixel array **102**. The outputs **118** are coupled to an output block **120** comprising active loads for driving each column line as well as switches for selecting columns, as will be described in more detail below.

In one embodiment, the columns are read in sequence, under control of a column decoder **122**. The column decoder **122** receives a column selection signal on input lines **124**. Assuming that the pixel array **102** comprises 32 columns, the column selection signal on line **124** is for example 5 bits wide. The column decoder **122** provides a corresponding control signal on output lines **126** to control one or more switches of the output block **120** associated with each column of the pixel array **102**.

The output block **120**, for example, provides an output on output lines **128**, of which there are one or more output lines associated with each column. The output block **120** provides an analog voltage level representing the values read from the pixel circuit of a selected row and column. The analog voltage values are for example provided to one or more output amplifier circuits. In the example of FIG. **1**, an example of an amplifier circuit comprising an amplifier **130**, for example an operational amplifier, is illustrated. A positive input of the amplifier **130** is coupled to the output lines **128**, and the negative input of amplifier **130** is coupled to the output lines **128** via a resistor **132**. The negative input is also coupled to the output of the amplifier **130** via a resistor **134**. The output of the amplifier **130** is further coupled to an analog to digital converter (ADC) **136**, which generates a digital value on output lines **138** based on the analog input voltage read from the pixel array **102**. For example, the ADC is a ramp converter, which is well known in the art.

In alternative embodiments, the columns could be read in parallel, an amplifier and an ADC being provided for each column.

Of course, the amplifier circuit at the output of the pixel array could be implemented in many different ways as will be appreciated by those skilled in the art, the circuit illustrated in FIG. **1** being only one example.

FIG. **2** schematically illustrates an example of one of the pixel circuits **104** of the pixel array **102** in more detail according to an example embodiment, along with column lines and output circuitry.

Each pixel circuit **104**, for example, comprises an antenna **202** having differential outputs coupled to a detector **204**. The detector **204** comprises transistors **206** and **208**, which are for example n-channel MOS (NMOS) transistors controlled at their gate nodes by a bias voltage V_{gate} on a line **207**. Transistor **206** is coupled by its main current terminals between an output terminal **209** of the antenna **202** and the gate node of a transistor **210**, which is for example a p-channel MOS (PMOS) transistor. Transistor **208** is coupled by its main current terminals between an output terminal **211** of the antenna **202** and the gate of a transistor **212**, which is for example a PMOS transistor. The source nodes of transistors **210** and **212** are coupled to the supply voltage V_{DD} via the main current terminals of a transistor **214**, which receives at its gate node a row selection signal R_{SEL} from the row decoder **106** of FIG. **1**.

The drain of transistor **210** is coupled to a first column line **216**, while the drain of transistor **212** is coupled to a second column line **218**. Thus the column lines **216** and **218** are both associated with a signal column of pixel circuits **104** of the pixel array **102**.

The column lines **216** and **218** provide a differential electrical operation mode output, and correspond to the output **118** of one column represented in FIG. **1**. These column lines **216**, **218** are coupled to each pixel circuit of the column, and to ground via current sources **220** and **222** respectively of the output block **120**. The output block **120** further comprises column selection transistors **224** and **226**, which are for example PMOS transistors. Transistor **224** is coupled between column line **216** and an output line **228**, while transistor **226** is coupled between column line **218** and an output line **230**. Transistors **224** and **226** are each for example controlled by a control signal C_{SEL} for example generated by block **122** of FIG. **1** and provided to the output block **120** via the lines **126**. The output lines **228**, **230** for example provide differential output signals COL_{OUT+} and COL_{OUT-}, which are differential electrical operation mode outputs corresponding to two of the lines **128** at the output of the output block **120** of FIG. **1**. Each output line **228**, **230** is for example coupled to the input of a corresponding amplifier circuit and ADC, for example similar to the amplifier **130** and ADC **136** of FIG. **1**.

The imager **100** of FIG. **1** is for example a heterodyne or homodyne imager. In other words, a frequency signal is for example mixed with the received terahertz image signal.

In the case of a homodyne imager, the frequency signal is for example substantially equal to the frequency of the terahertz image signal, for example to the frequency of an illuminating terahertz signal. For example, the scene is illuminated by a transmission at a frequency of between 600 GHz and 1 THz, and a frequency signal of the same frequency is mixed with the received terahertz image signal. For example, the scene is illuminated by a transmission at a frequency of 650 GHz, and the frequency of the frequency signal is also 650 GHz.

In the case of a heterodyne imager, the frequency signal is for example chosen to be different from the frequency of the terahertz image signal. For example, assuming that the scene is illuminated by a transmission at a frequency of between 600 GHz and 1 THz, the frequency signal has a frequency different to that of the illumination frequency by between 1 and 5 GHz. As an example, the scene could be illuminated by a transmission at a frequency of 650 GHz, and the frequency of the frequency signal is of 649 or 651 GHz.

Due at least in part to its high frequency, there is a technical difficulty in applying the frequency signal to the detector **204** of the pixel circuit. Indeed, MOS transistors have a maximum operating frequency f_T above which the gain of the transistor falls very low. The frequency f_T of a typical MOS transistor is at around 200 GHz for 65 nm technology, which is significantly lower than the terahertz frequency range. Furthermore, the frequency signal must be supplied to each pixel circuit on a particularly low resistance path.

As illustrated in FIG. **2**, the frequency signal f_{LO} from a local oscillator **232** of the frequency oscillator circuit **115** is coupled via the line **116** to an input terminal **234** of the antenna. The input terminal **234** is for example an input of the antenna usually associated with a biasing voltage of the antenna. The frequency signal for example also includes a DC bias. The terminal **234** is adapted to be of equal distance from each of the differential outputs **209**, **211** of the antenna. Thus the frequency signal is applied in a balanced manner to each input of the detector **204**. The combination of the antenna **202** and the detector **204** formed of the transistors **206** and **208** forms a mixer, mixing the frequency signal f_{LO} with the received terahertz signal.

In one example, a single frequency oscillator circuit **115** comprising one or more oscillators **232** provides a frequency signal for all of the pixel circuits of the array. Alternatively, there may be more than one frequency oscillator circuit **115**, each for example providing the frequency signal to a different group of pixel circuits.

FIG. **3** illustrates the pixel circuit **104** and output circuitry according to an alternative embodiment. Those features in common with the embodiment of FIG. **2** have been labeled with like reference numerals and will not be described again in detail.

In the embodiment of FIG. **3**, the transistors **206** and **208** of the detector **204** are coupled respectively between the nodes **209** and **211** of the antenna **202** and a common output node **302** of the pixel circuit. The output node **302** is coupled to a grounded capacitor **304** and also to the gate node of PMOS transistor **210**. The row selection transistor **214**, current source **220** and column selection transistor **224** are the same as those of the pixel circuit of FIG. **2**, and will not be described again in any detail. The second set of column output components **212**, **222** and **226** are not present in the pixel circuit of FIG. **3**, a single output line being provided from each column.

The pixel circuit of FIG. **3** is, for example, a homodyne circuit as described above. With respect to a similar pixel circuit without an input receiving the frequency signal f_{LO} the circuit of FIG. **3** is more sensitive to the terahertz image signal, which generally leads to a quality improvement.

FIG. **4** is a plan view of the antenna **202** of the pixel circuit **104** of FIG. **2** in more detail. As illustrated, the antenna for example comprises an inner conductive ring **402** formed within a larger circular zone **404** of a substrate, which is for example a zone in which the substrate is covered by an epi layer blocker.

The input terminal **234** of the antenna is formed as a protrusion at a point on the outer edge of the ring **402**. The frequency signal f_{LO} is applied at an extremity of a conducting track **116** connected to the terminal **234**.

The differential output terminals **209** and **211** of the antenna are for example formed as protrusions from the inner edge of the ring **402**, on opposite sides. The points at which the output terminals **209** and **211** are formed are each at the same distance from the input terminal **234**. The detector **204** is for example formed in a central zone surrounded by the ring **402**. Conducting tracks **406** and **408** for example bring the differential output signals IF+ and IF− to the corresponding column lines (not illustrated in FIG. **4**). In some embodiments, the transistors **210**, **212** and **214** are also formed in the central zone surrounded by ring **402**.

The ring **402** for example has an average diameter of between 50 and 200 μm, and the thickness of the ring between its inner and outer edges is for example between 5 and 25 μm.

The antenna of the embodiment of FIG. **3** is for example formed of the same circuit as FIG. **4**, except that a single output track from the detector **204** is present.

FIG. **5** illustrates a frequency oscillation circuit **500** according to an example embodiment. The circuit **500** is for example used to implement the frequency oscillation circuit **115** of FIGS. **2** and **3**. Alternatively, the frequency oscillator circuit **500** may have other applications, such as providing a high frequency signal for generating terahertz radiation, for example for illuminating a scene to be captured by a terahertz imager.

As indicated above, a difficulty in processing terahertz signals by MOS transistors is that the maximum operating transistor frequency f_T of a MOS transistor is far lower than the terahertz frequency range.

To overcome this difficulty, the circuit **500** comprises a ring oscillator formed of an odd number of series-coupled inverters coupled in a loop, each of the inverters operating within the frequency limit of MOS technology, for example at between 150 to 200 GHz in the case 65 nm technology. In the example of FIG. **5**, three inverters are formed by NMOS transistors **502**, **504** and **506**. The transistor **502** is coupled between a node **508** and ground, for example having its source connected to ground, and its drain connected to node **508**. Node **508** is further coupled via an inductor **510** to the gate node of the transistor **504**. Similarly, transistor **504** is coupled between a node **512** and ground, node **512** further being coupled via an inductor **514** to the gate node of transistor **506**. Transistor **506** is coupled between node **516** and ground, node **516** being coupled to the gate of transistor **502** via an inductor **518**.

The node **508** is further coupled via an inductor **520**, or other form of band-pass filter, to a summing node **522**. Similarly, nodes **512** and **516** are coupled to the summing node **522** via inductors **524** and **526** respectively, or other forms of pass band filters. The summing node **522** is supplied by a voltage source **528** coupled to the summing node **522** via an inductor **530**. For example the voltage source provides a DC bias voltage of between 0.5 and 2.5 V.

The summing node **522** is coupled via an inductor **532** to an output node **534** of the frequency oscillator circuit **500**. The node **534** is also for example coupled to ground via a resistor **536**.

As represented in FIG. **5**, in some embodiments the chain of inverters is extended to comprise more than three inverters and corresponding inductors, for example any odd number.

For example, the chain of inverters could comprise 5, 7 or 9 inverters and corresponding inductors.

Operation of the circuit **500** of FIG. **5** will now be described in more detail with reference to FIGS. **6** and **7**. In this example, the inverter chain comprises three inverters.

FIG. **6** is a graph showing a frequency spectrum of the signal present at each of the nodes **508**, **512** and **516** of FIG. **5**. The signal at each of these nodes is a square wave comprising various sinusoidal components. In particular, the signal is composed of a wave of amplitude A at a fundamental frequency f. The fundamental frequency depends on the number of transistors in the loop, and the delay introduced by each transistor. A typical example of such frequency could be between 150 GHz to 200 GHz. Furthermore, the signal comprises waveforms at the odd harmonic frequencies. FIG. **6** illustrates the third harmonic having an amplitude A/3, the fifth harmonic having an amplitude A/5 and the seventh harmonic having an amplitude A/7.

Assuming a fundamental frequency at between 150 and 200 GHz, the third harmonic is for example at between 450 and 600 GHz, and the fifth harmonic is for example at between 750 GHz and 1 THz. The seven harmonic is for example at between 1 THz and 1.4 THz.

Each of the inductors **520**, **524** and **526**, which couple the nodes **508**, **514** and **516** to the summing node **522**, is selected to provide a band-pass filter having the pass band centre indicated by a dashed line in FIG. **6**, to select the third harmonic frequency signal. For example, in the case of selecting the third harmonic frequency, the pass band is for example between 400 and 700 GHz, and the inductors **520**, **524** and **526** for example each have a value of a few pH or less.

In the more general case of a ring oscillator having N inverters, N being an odd integer equal to 3 or more, the pass bands of the filters coupling the output of each inverter to the summing node are for example chosen to select the Nth harmonic frequency. In such a ring oscillator of N inverters, the Nth harmonic has the property of being in phase at the output node of each inverter, as will now be explained with reference to FIG. **7**.

FIG. **7** shows three graphs showing examples of the fundamental frequency signal **702** and Nth harmonic frequency **704** present at nodes **508**, **512** and **516** respectively, for the case that N is equal to three.

As illustrated, the phase of the fundamental frequency **702** is shifted at each node with respect to the previous node by $2\pi/N$ radians, and the signal is inverted. This makes the fundamental frequency signal present at each node unsuitable for being combined. However, due to its higher frequency, the same shift in the Nth harmonic frequency (third harmonic in the example of FIG. **7**) results in in-phase waveforms at each node **508**, **512** and **516**. Thus, the Nth harmonic frequencies add with constructive interference to generate a signal of higher amplitude. Furthermore, the frequency of the Nth harmonic frequency is N times that of the fundamental frequency, allowing the maximum transistor frequency f_T of the transistor technology to be exceeded.

FIG. **8** is a plan view illustrating the layout structure of a frequency oscillation circuit **800** according to a further embodiment.

In the example of FIG. **8**, there are two rings oscillators **801** and **802**, each formed in a similar fashion to the circuit of FIG. **5**, and each comprising 5 inverters.

In particular, ring oscillator **801** comprises inverters **803**, **804**, **805**, **806** and **807** coupled in a ring in a similar fashion to the inverters **502**, **504** and **506** of FIG. **5**. The connections between the inverters are formed by transmission lines, which also form the role of the inductors. Each of the inverters is further coupled by a corresponding transmission line of equal length to a node **808** forming the summing node **522** of the ring oscillator **801**, these transmission lines forming inductors of the band-pass filters. A transmission line **809** from the summing node **808** provides the summed frequency signal.

Similarly, the ring oscillator **802** comprises inverters **813**, **814**, **815**, **816** and **817** coupled in a ring in a similar fashion to the inverters **502**, **504** and **506** of FIG. **5**. The connections between the inverters are formed by transmission lines, which also form the role of the inductors. Each of the inverters is further coupled to a node **818** forming the summing node **522** of the ring oscillator **802**. A transmission line **819** from the summing node **818** provides the summed frequency signal.

Each of the transmission lines **809**, **819** is electromagnetically coupled to a common output track **820**, which provides the resulting frequency signal f_{LO}.

In order for the frequency signal generated by each of the ring oscillators to be summed on the output track **820**, they should be in-phase. To achieve this, electromagnetic coupling is provided between the ring oscillators **801**, **802**, and in particular between at least one of the transmission lines between inverters of each ring oscillator. In the example of FIG. **8**, the transmission line coupling inverters **804** and **805** is electromagnetically coupled to the transmission line coupling inverters **814** and **815**. For example, to achieve phase synchronisation, there is between −5 and −15 dB of cross-coupling between the lines. Those skilled in the art will understand how to achieve a desired level of cross-coupling, based for example on the spacing between the transmission lines.

FIG. **9** illustrates a frequency oscillation circuit **900** according to a further embodiment. In this example, six ring oscillators **902**, **904**, **906**, **908**, **910** and **912** are each coupled in relatively close proximity. Furthermore, an output line from each of the ring oscillators **902** to **912** is electromagnetically coupled to a common conductive track **914**, which for example makes a horse shoe shape surrounding the ring oscillators and provides the output frequency signal f_{LO} at output terminals **916** and **918** at its respective extremities. Each of the ring oscillators is electromagnetically coupled to at least two of the other ring oscillators in similar fashion to the oscillators **801** and **802** of FIG. **8**.

Optionally, a further conductive track **920** may be provided passing by a transmission line of each ring oscillator **902** to **912**, such that a further oscillation frequency can be used to tune the frequency and phase oscillation of each oscillator. For example, the further oscillation frequency signal is generated by a main phase-locked and frequency-tunable oscillator **924**, which locks to a further high frequency oscillator **922**.

As represented by a series of dots in FIG. **9**, while 6 ring oscillators are represented in FIG. **9**, the principle could be extended to a greater number of oscillators.

It will be apparent to those skilled in the art that, the higher the number of ring oscillators operating in phase, the higher the output amplitude of the generated frequency signal. For example, a high amplitude signal can be beneficial for transmitting terahertz radiation to illuminate a scene, or for having enough power for the signal to be provided to all of the pixel circuits of a heterodyne or homodyne image sensor.

FIG. **10** illustrates a terahertz device **1000**, which for example comprises a frequency oscillation circuit **1002** for generating a frequency signal f_{LO}. The frequency signal is for example provided to a transmission system **1004** for illuminating a scene and/or to a terahertz image sensor **1006** for capturing a scene using a heterodyne or homodyne imager.

An advantage of the embodiments described herein with reference to FIGS. **2**, **3** and **4** is that a simple pixel circuit can be provided in which a frequency signal is mixed with a received terahertz image signal.

An advantage of the embodiments described herein with reference to FIGS. **5** to **9** is that a high frequency signal can be generated without being limited by the maximum transistor frequency f_T of the transistor technology that is used.

Having thus described at least one illustrative embodiment of the invention, various alterations, modifications and improvements will readily occur to those skilled in the art.

For example, while in the embodiment of FIG. **4** an example shape and layout of an antenna has been represented, it will be apparent to those skilled in the art that various different shapes and layouts could be used.

Furthermore, while in the examples of FIGS. **5** to **9** the output of each inverter of each ring oscillator is summed to generate the output signal, it would be possible to sum only the output taken from two or more of the inverters. However, there is of course an interest in summing the maximum number of signals if the objective is to generate an output signal of the highest amplitude.

What is claimed is:

1. A frequency oscillator comprising:

a first ring oscillator having N inverters coupled in series, where N is an odd integer equal to three or more;

a first filter coupled between an output node of a first of the inverters and an output line of the frequency oscillator; and

a second filter coupled between an output node of a second of the inverters and the output line of the frequency oscillator, wherein the first and second filters each have a lower cut-off frequency falling between the (N−2)th and the Nth harmonic present at the outputs of the inverters and a higher cut-off frequency falling between the Nth and (N+2)th harmonic present at the outputs of the inverters.

2. The frequency oscillator of claim **1**, wherein the frequency oscillator further comprises a second ring oscillator formed of N inverters coupled in series, wherein at least one line connecting a pair of inverters of the first ring oscillator is positioned to be electro-magnetically coupled to at least one line connecting a pair of inverters of the second ring oscillator.

3. The frequency oscillator of claim **1**, wherein N is equal to 5 or 7.

4. The frequency oscillator of claim **1**, wherein the first filter comprises a first inductor and the second filter comprises a second inductor.

5. The frequency oscillator of claim **1**, wherein an output of at least one of the N inverters is coupled to the input of the next inverter via a further inductor.

6. The frequency oscillator of claim **1**, wherein a frequency signal on the output line has a frequency in the range of 300 GHz to 3 THz.

7. The frequency oscillator of claim **6**, wherein a signal at the output node of the first of the inverters is half or smaller than the frequency of the frequency signal on the output line.

8. The frequency oscillator of claim **6**, wherein each of the inverters comprises a transistor having a gate length of 65 nm or smaller.

9. A method of generating a frequency signal, the method comprising:

generating an oscillating signal using a ring oscillator having N inverters coupled in series, where N is an odd integer equal to three or more, the oscillating signal generated at an output of each of the inverters;

filtering the oscillating signal at the output of at least two of the inverters to extract the Nth harmonic, wherein filtering comprises band-pass filtering around the Nth harmonic, and wherein band-pass filtering includes a lower cut-off frequency falling between the (N−2)th and the Nth harmonic present at the output of at least two of the inverters and a higher cut-off frequency falling between the Nth and (N+2)th harmonic present at the output of at least two of the inverters; and

combining the filtered oscillating signals to generate an output frequency signal.

10. The method of claim **9**, further comprising generating a further oscillating signal using a further ring oscillator having N inverters coupled in series, the further oscillating signal being generated at the output of each of the inverters, wherein at least one line connecting a pair of inverters of the ring oscillator is positioned to be electro-magnetically coupled to at least one line connecting a pair of inverters of the further ring oscillator;

filtering the oscillating signal at the output of at least two of the inverters of the further ring oscillator to extract the Nth harmonic; and

combining the filtered oscillating signals of the further ring oscillator with the filtered oscillating signals of the ring oscillator to generate the output frequency signal.

11. The method of claim **9**, wherein the ring oscillator further comprises a first filter coupled between an output node of a first of the inverters and an output line of the ring oscillator and a second filter coupled between an output node of a second of the inverters and the output line of the ring oscillator.

12. The method of claim **11**, wherein the first filter comprises a first inductor and the second filter comprises a second inductor.

13. The method of claim **9**, wherein N is equal to 5 or 7.

14. The method of claim **9**, wherein the output frequency signal has a frequency in the range of 300 GHz to 3 THz.

15. A terahertz frequency oscillator comprising:

a first transistor having a source, a drain and a gate, the first transistor having a gate length of 65 nm or smaller, the gate of the first transistor being coupled to a drain of an Nth transistor, where N is an odd integer equal to three or more;

a second transistor having a source, a drain and a gate, the second transistor having a gate length of 65 nm or smaller, the gate of the second transistor being coupled to the drain of the first transistor;

a third transistor having a source, a drain and a gate, the third transistor having a gate length of 65 nm or smaller, the gate of the third transistor being coupled to the drain of the second transistor;

a first inductor coupled between the drain of the first transistor and an output line;

a second inductor coupled between the drain of the second transistor and the output line;

a third inductor coupled between the drain of the third transistor and the output line; and

a ground node, wherein the sources of the first, second and third transistors are coupled to the ground node;

wherein the frequency oscillator is configured to carry an output frequency signal having a frequency in the range of 300 GHz to 3 THz at the output line.

16. A terahertz frequency oscillator comprising:

a first transistor having a source, a drain and a gate, the first transistor having a gate length of 65 nm or smaller, the gate of the first transistor being coupled to a drain of an Nth transistor, where N is an odd integer equal to three or more;

a second transistor having a source, a drain and a gate, the second transistor having a gate length of 65 nm or smaller, the gate of the second transistor being coupled to the drain of the first transistor;

a third transistor having a source, a drain and a gate, the third transistor having a gate length of 65 nm or smaller, the gate of the third transistor being coupled to the drain of the second transistor;

a first inductor coupled between the drain of the first transistor and an output line;

a second inductor coupled between the drain of the second transistor and the output line;

a third inductor coupled between the drain of the third transistor and the output line; and

a voltage source coupled to the output line through a fourth inductor;

wherein the frequency oscillator is configured to carry an output frequency signal having a frequency in the range of 300 GHz to 3 THz at the output line.

17. A terahertz frequency oscillator comprising:

a first transistor having a source, a drain and a gate, the first transistor having a gate length of 65 nm or smaller, the gate of the first transistor being coupled to a drain of an Nth transistor, where N is an odd integer equal to three or more;

a second transistor having a source, a drain and a gate, the second transistor having a gate length of 65 nm or smaller, the gate of the second transistor being coupled to the drain of the first transistor;

a third transistor having a source, a drain and a gate, the third transistor having a gate length of 65 nm or smaller, the gate of the third transistor being coupled to the drain of the second transistor;

a first inductor coupled between the drain of the first transistor and an output line;

a second inductor coupled between the drain of the second transistor and the output line;

a third inductor coupled between the drain of the third transistor and the output line;

a fourth inductor coupled between the gate of the first transistor and the drain of the Nth transistor;

a fifth inductor coupled between the gate of the second transistor and the drain of the first transistor; and

a sixth inductor coupled between the gate of the third transistor and the drain of the second transistor;

wherein the frequency oscillator is configured to carry an output frequency signal having a frequency in the range of 300 GHz to 3 THz at the output line.

18. The frequency oscillator of claim **15**, wherein N is equal to 3 so that the third transistor is the Nth transistor.

19. The frequency oscillator of claim **15**, wherein N is equal to 5 or 7.

20. The frequency oscillator of claim **17**, wherein N is equal to 5 or 7.

21. The frequency oscillator of claim **17**, wherein N is equal to 3 so that the third transistor is the Nth transistor.

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